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1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - Apps www.analog.com/MicroConverter

4 ;

5 ; Date : October 2003

6 ;

7 ; File : ADCtimer.asm

8 ;

9 ; Hardware : ADuC842/ADuC843

10 ;

11 ; Description : Performs ADC conversions at 116KSPS in Timer2 mode.

12 ; Outputs ADC results to RAM. Continuously

13 ; flashes LED (independently of ADC routine) at

14 ; approximately 3Hz.

15 ; All rate calculations assume an 2.097152MHz Mclk.

16 ;

17 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

18

19 $MOD842 ; Use 8052&ADuC842 predefined symbols

20

00B4 21 LED EQU P3.4 ; P3.4 drives red LED on eval board

0000 22 CHAN EQU 0 ; convert this ADC input channel..

23 ; ..chan values can be 0 thru 6

24

---- 25 DSEG

0030 26 ORG 0030H

0028 27 LENGTH EQU 40

0030 28 BUFFER: DS LENGTH ; set up buffer in RAM

29

30 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

31 ; BEGINNING OF CODE

---- 32 CSEG

33

0000 34 ORG 0000h

35

0000 02004B 36 JMP MAIN ; jump to main program

37 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

38 ; INTERRUPT VECTOR SPACE

0033 39 ORG 0033H ; (ADC ISR)

0033 B85803 40 CJNE R0,#58H,CONT

0036 02003F 41 JMP EXIT ; place breakpoint here to view ram in debugger after conver

sions

0039 A6DA 42 CONT: MOV @R0,ADCDATAH

003B 08 43 INC R0

003C A6D9 44 MOV @R0,ADCDATAL

003E 08 45 INC R0

003F 32 46 EXIT: RETI

47

48

49 ;====================================================================

50 ; MAIN PROGRAM

004B 51 ORG 004Bh

52

004B 7830 53 MAIN: MOV R0,#BUFFER

54 ; PRECONFIGURE...

004D 75EF9E 55 MOV ADCCON1,#09Eh ; power up ADC & enable Timer2 mode

0050 75D800 56 MOV ADCCON2,#CHAN ; select channel to convert

0053 75CAF6 57 MOV RCAP2L,#0F6h ; sample period = 2 \* T2 reload prd

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0056 75CBFF 58 MOV RCAP2H,#0FFh ; = 2\*(10000h-FFF6h)\*0.476us

0059 75CCF6 59 MOV TL2,#0F6h ; = 2\*9\*0.476us

005C 75CDFF 60 MOV TH2,#0FFh ; = 8.5us

61

62 ; LAUNCH Timer2 DRIVEN CONVERSIONS...

005F D2AF 63 SETB EA ; enable interrupts

0061 D2AE 64 SETB EADC ; enable ADC interrupt

0063 D2CA 65 SETB TR2 ; run Timer2

66

67 ; CONTINUE WITH OTHER CODE...

0065 B2B4 68 AGAIN: CPL LED ; blink (complement) the LED

0067 740A 69 MOV A,#010 ; Delay length

0069 12006E 70 CALL DELAY ; delay 100ms

006C 80F7 71 JMP AGAIN ; repeat

72

73 ; the micro is free to continue with other tasks (flashing the LED in

74 ; this case) while the ADC operation is being controlled by Timer2

75 ; and the ADC interrupt service routine.

76

77 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

78 ; SUBROUTINE

006E 79 DELAY: ; Delays by 10ms \* A

80 ; 10mSec based on 2.09MHZ

81 ; Core Clock

82 ; i.e. default ADuC842 Clock

83

006E F9 84 MOV R1,A ; Acc holds delay variable (1 clock)

006F 7A1B 85 DLY0: MOV R2,#01Bh ; Set up delay loop0 (2 clocks)

0071 7BFF 86 DLY1: MOV R3,#0FFh ; Set up delay loop1 (2 clocks)

0073 DBFE 87 DJNZ R3,$ ; Dec R3 & Jump here until R3 is 0 (3 clocks)

0075 DAFA 88 DJNZ R2,DLY1 ; Dec R2 & Jump DLY1 until R2 is 0 (3 clocks)

0077 D9F6 89 DJNZ R1,DLY0 ; Dec R1 & Jump DLY0 until R1 is 0 (3 clocks)

0079 22 90 RET ; Return from subroutine

91

92 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

93

94 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

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ADCCON1. . . . . . . . . . . . . D ADDR 00EFH PREDEFINED

ADCCON2. . . . . . . . . . . . . D ADDR 00D8H PREDEFINED

ADCDATAH . . . . . . . . . . . . D ADDR 00DAH PREDEFINED

ADCDATAL . . . . . . . . . . . . D ADDR 00D9H PREDEFINED

AGAIN. . . . . . . . . . . . . . C ADDR 0065H

BUFFER . . . . . . . . . . . . . D ADDR 0030H

CHAN . . . . . . . . . . . . . . NUMB 0000H

CONT . . . . . . . . . . . . . . C ADDR 0039H

DELAY. . . . . . . . . . . . . . C ADDR 006EH

DLY0 . . . . . . . . . . . . . . C ADDR 006FH

DLY1 . . . . . . . . . . . . . . C ADDR 0071H

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EADC . . . . . . . . . . . . . . B ADDR 00AEH PREDEFINED

EXIT . . . . . . . . . . . . . . C ADDR 003FH

LED. . . . . . . . . . . . . . . NUMB 00B4H

LENGTH . . . . . . . . . . . . . NUMB 0028H

MAIN . . . . . . . . . . . . . . C ADDR 004BH

P3 . . . . . . . . . . . . . . . D ADDR 00B0H PREDEFINED

RCAP2H . . . . . . . . . . . . . D ADDR 00CBH PREDEFINED

RCAP2L . . . . . . . . . . . . . D ADDR 00CAH PREDEFINED

TH2. . . . . . . . . . . . . . . D ADDR 00CDH PREDEFINED

TL2. . . . . . . . . . . . . . . D ADDR 00CCH PREDEFINED

TR2. . . . . . . . . . . . . . . B ADDR 00CAH PREDEFINED